

1 CLAIMS:

2 1. A method of forming integrated circuit devices comprising:
3 forming a plurality of patterned device outlines over a
4 semiconductive substrate;

5 forming electrically insulative spacers on at least a portion of the
6 patterned device outlines; and

7 forming a plurality of substantially identically shaped devices
8 relative to the patterned device outlines, at least two individual devices
9 of the plurality being spaced from one another by a distance no greater
10 than a width of an interposed electrically insulative spacer.

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12 2. The method of forming integrated circuit devices of claim 1,
13 wherein the devices are elongated electrically conductive lines.

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15 3. The method of forming integrated circuit devices of claim 1,
16 wherein the devices include capacitors of a DRAM array.

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18 4. The method of forming integrated circuit devices of claim 1,
19 wherein the plurality of devices are formed along a line, respective
20 alternate devices along the line having a substantially common width
21 dimension.

1 5. The method of forming integrated circuit devices of claim 1,
2 wherein the plurality of devices are formed along a line, respective
3 adjacent devices along the line having different width dimensions.

4 6. The method of forming integrated circuit devices of claim 1,
5 wherein the devices include capacitors of a DRAM array, the capacitors
6 being formed in rows, respective alternate capacitors in a row having
7 substantially similar width profiles transverse the row.

8 7. The method of forming integrated circuit devices of claim 1,
9 wherein the devices include capacitors of a DRAM array, the capacitors
10 being formed in rows, adjacent capacitors in a row having different
11 width profiles transverse the row.

12 8. The method of forming integrated circuit devices of claim 1,
13 wherein the devices include capacitors of a DRAM array, the capacitors
14 being formed in rows, respective alternate capacitors in a row having
15 substantially similar width profiles transverse the row, adjacent capacitors
16 in the row having different width profiles transverse the row.

1 9. A method of forming a plurality of integrated circuitry
2 devices on a substrate comprising:

3 forming a plurality of spaced, upstanding, anisotropically etched
4 electrically insulative spacers; and

5 forming a plurality of devices over the substrate intermediate the
6 spacers with the spacers being positioned intermediate adjacent devices,
7 adjacent devices having a pitch which is substantially no greater than
8 about the distance between a pair of adjacent spacers plus the width
9 of the spacer between the adjacent devices.

10 10. The method of forming a plurality of integrated circuitry
11 devices of claim 9, wherein the devices are conductive) lines.

13 11. The method of forming a plurality of integrated circuitry
14 devices of claim 9, wherein the devices are capacitors.

16 12. The method of forming a plurality of integrated circuitry
17 devices of claim 9, wherein the devices are capacitors of a DRAM
18 device.

1 13. A DRAM capacitor forming method comprising the steps of:
2 forming a plurality of patterned outlines over a semiconductive
3 substrate to define individual areas for a plurality of capacitors to be
4 formed;

5 partitioning said individual areas from one another by a non-
6 conducting partition; and

7 forming capacitors in at least some of the respective partitioned
8 areas, the respective capacitors being separated from immediately
9 adjacent capacitors by a distance substantially no greater than the width
10 of the partition therebetween.

11 14. The DRAM capacitor forming method of claim 13, wherein
12 the partitioning step comprises:

13 etching a first set of capacitor container openings, individual
14 container openings having at least one upright sidewall; and

15 etching a second set of capacitor container openings adjacent
16 respective first set container openings and separated therefrom by
17 respective non-conducting partitions.

1 15. The DRAM capacitor forming method of claim 13, wherein
2 the partitioning step comprises:

3 etching a first set of capacitor container openings, individual
4 container openings having at least one upright sidewall;

5 forming insulative material over the substrate;

6 anisotropically etching the insulative material to provide partitions
7 over at least some of the upright sidewalls; and

8 etching a second set of capacitor container openings immediately
9 adjacent the provided partitions.

10
11 16. The DRAM capacitor forming method of claim 13 wherein
12 individual defined areas, when viewed from a point above the substrate,
13 approximate diamond shapes.

14
15 17. A DRAM capacitor forming method comprising the steps of:
16 forming a pair of adjacent capacitor containers over a substrate
17 by etching a first capacitor container opening having at least one
18 upright sidewall;

19 forming an electrically insulative spacer on the upright sidewall;

20 selectively etching a second capacitor container opening adjacent
21 the formed spacer;

22 forming capacitors in the capacitor containers, adjacent capacitors
23 having a separation distance therebetween which is substantially no
24 greater than the width of the spacer between the adjacent capacitors.

1 18. The DRAM capacitor forming method of claim 17, wherein
2 the step of forming the electrically insulative spacer comprises:
3 forming an insulative material over the substrate; and
4 anisotropically etching the insulative material to form the spacer.
5

6 19. The DRAM capacitor forming method of claim 17, wherein
7 individual capacitor containers are generally triangularly shaped when
8 viewed from a point above the substrate.
9

10 10 20. A method of forming capacitors comprising forming an array
11 of capacitor pairs on a substrate, the array being defined in part by a
12 plurality of lines, individual lines containing at least one pair of
13 capacitors, individual capacitors of said at least one pair of capacitors
14 being separated by substantially no more than an electrically insulative
15 anisotropically etched spacer disposed therebetween.
16

17 17 21. The method of forming capacitors of claim 20 further
18 comprising prior to forming the array of capacitor pairs, forming a
19 plurality of bit line contacts in individual lines, individual capacitor pairs
20 being bounded by at least two bit line contacts.
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1 22. The method of forming capacitors of claim 20 wherein
2 individual capacitor pairs have a pitch no greater than about a lateral
3 width dimension of one of the capacitors plus the width of the
4 anisotropically etched spacer between the capacitors of an individual
5 pair.

6
7 23. A DRAM capacitor array comprising:
8 a substrate;
9 a first set of capacitors over the substrate; and
10 a second set of capacitors over the substrate, individual capacitors
11 of the first set being bounded by at least three capacitors from the
12 second set, individual first set capacitors having a closest separation
13 distance from at least one of the three capacitors from the second set
14 which is substantially no more than a width of an interposed electrically
15 insulative anisotropically etched spacer.

16
17 24. The DRAM capacitor array of claim 23, wherein individual
18 bounded first set capacitors have closest separation distances from no
19 less than two of the three capacitors from the second set, said closest
20 separation distances being substantially no more than a width of an
21 interposed electrically insulative anisotropically etched spacer.

25. The DRAM capacitor array of claim 23, wherein individual bounded first set capacitors have closest separation distances from the three capacitors from the second set which are substantially no more than a width of an interposed electrically insulative anisotropically etched spacer.

26. A method of forming a plurality of capacitors in a semiconductor memory device comprising the steps of:

selectively removing substrate material to define a first set of containers;

forming sidewall spacers adjacent container sidewalls;

selectively removing remaining substrate material adjacent the spacers to define a second set of containers; and

forming capacitors in the containers separated only by the spacers.

27. The method of forming a plurality of capacitors of claim 26 further comprising prior to defining the first set of containers:

forming a plurality of bit line contact openings over the substrate, individual bit line contact openings having at least one sidewall; and

covering the at least one sidewall of the plurality of bit line contact openings with an insulating material.

1 28. The method of forming a plurality of capacitors of claim 26
2 further comprising prior to defining the first set of containers:

3 forming a plurality of bit line contact openings over the substrate,
4 individual bit line contact openings having at least one sidewall;

5 covering the at least one sidewall of the plurality of bit line
6 contact openings with an insulating material;

7 etching the insulating material to form sidewall spacers; and

8 forming electrically conductive material in the bit line contact
9 openings to provide bit line contacts,

10 wherein the defining of the first set of containers includes
11 selectively etching the first set of containers relative to the sidewall
12 spacers and the electrically conductive material of the bit line contacts.

14 29. A DRAM capacitor forming method comprising forming a
15 plurality of pairs of adjacent capacitors in respective adjacent capacitor
16 containers separated by substantially no more than anisotropically etched
17 sidewall spacers.

19 30. The DRAM capacitor forming method of claim 29, wherein
20 individual pairs of adjacent capacitors, when viewed from a point over
21 the substrate are approximately diamond shaped.

1 31. The DRAM capacitor forming method of claim 29 further
2 comprising forming a plurality of bit line contact openings over the
3 substrate prior to forming the capacitor pairs.

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5 32. The DRAM capacitor forming method of claim 29 further
6 comprising forming a plurality of bit line contact openings over the
7 substrate prior to forming the capacitor pairs, and wherein individual
8 pairs of adjacent capacitors, when viewed from a point over the
9 substrate are approximately diamond shaped, individual bit line contact
10 openings being positioned in respective corners of the diamonds.

11

12 33. A capacitor array for a DRAM comprising:
13 a plurality of bit line contacts to a substrate; and
14 a plurality of capacitor pairs selectively alternately etched over a
15 substrate along etch axes which are generally orthogonal relative to the
16 substrate, individual capacitor pairs having an area which, when viewed
17 from outwardly of the substrate from a point on such etch axes,
18 approximates a parallelogram which is bounded at a plurality of its
19 corners by individual bit line contacts.

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1 34. A processing method of forming a capacitor array for a
2 DRAM comprising:

3 forming a plurality of bit line contacts to a substrate; and
4 forming a plurality of capacitor pairs, individual pairs being
5 selectively alternately etched over a substrate and along etch axes which
6 are generally orthogonal relative to the substrate, individual capacitor
7 pairs having an area which, when viewed from outwardly of the
8 substrate from a point on such etch axes, approximates a parallelogram
9 which is bounded at a plurality of its corners by individual bit line
10 contacts.

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12 35. A method of forming a plurality of DRAM capacitors
13 comprising:

14 etching capacitor container openings for an array in a substrate
15 in at least two separate etching steps, and forming electrically insulative
16 partitions between adjacent capacitors intermediate the two etching steps.

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18 36. The method of claim 35 wherein the forming electrically
19 insulative partitions step comprises:

20 forming insulative material over the substrate; and
21 conducting an anisotropic etch of the insulative material to a
22 degree sufficient to leave the partitions.

1 37. A processing method of forming a plurality of DRAM
2 capacitors comprising etching capacitor container openings for a capacitor
3 array in a substrate in two separate etching steps.

4
5 38. A DRAM capacitor array comprising:
6 a plurality of 6-capacitor geometries over a substrate, individual
7 6-capacitor geometries being defined by a plurality of individual generally
8 polygonal capacitor geometries, and

9 further, individual 6-capacitor geometries, when viewed from above
10 the substrate, approximating a hexagon, each individual side of which
11 being defined by a side of a different respective one of the individual
12 polygonal capacitor geometries.

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14 39. The DRAM capacitor array of claim 38, wherein individual
15 polygonal capacitor geometries, when viewed from above the substrate
16 approximate a wedge shape.

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18 40. The DRAM capacitor array of claim 38, wherein individual
19 polygonal capacitor geometries, when viewed from above the substrate
20 approximate a triangle.

21
22 41. The DRAM capacitor array of claim 38, wherein individual
23 polygonal capacitor geometries, when viewed from above the substrate
24 approximate an isosceles triangle.

1 42. The DRAM capacitor array of claim 38, wherein individual
2 polygonal capacitor geometries, when viewed from above the substrate
3 approximate an isosceles triangle equal adjacent angles of which
4 approximate a range of between about 50° to 70°.

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6 43. The DRAM capacitor array of claim 38, wherein individual
7 polygonal capacitor geometries, when viewed from above the substrate
8 approximate an isosceles triangle equal adjacent angles of which
9 approximate about 65°.

10
11 44. The DRAM capacitor array of claim 38, wherein the
12 hexagon can be bisected into halves containing exactly three individual
13 polygonal capacitor geometries.

14
15 45. A DRAM capacitor array comprising:
16 a plurality of 3-capacitor geometries over a substrate, individual
17 3-capacitor geometries, when viewed from above the substrate being
18 defined by a pair of overlapping approximated parallelograms, the
19 intersection of which approximates a triangle.

1 46. A method of forming adjacent devices over a substrate
2 comprising:

3 lithographically forming an array of patterned device outlines over
4 a substrate, the outlines defining alternating male/female patterns;

5 forming electrically insulative sidewall spacers in the female
6 patterns;

7 after forming the electrically insulative sidewall spacers, removing
8 the male patterns; and

9 after removing the male patterns, forming circuit devices adjacent
10 the spacers.

11
12 47. An integrated device array of substantially identically shaped
13 devices comprising:

14 a plurality of spaced upstanding anisotropically etched electrically
15 insulative spacers; and

16 a plurality of devices formed over the substrate intermediate the
17 spacers with the spacers being positioned intermediate adjacent devices,
18 adjacent devices having a pitch which is substantially no greater than
19 about the distance between a pair of adjacent spacers plus the width
20 of the spacer between the adjacent devices.

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22 48. The integrated device array of claim 47, wherein the devices
23 are conductive lines.

1 49. The integrated device array of claim 47, wherein the devices
2 are capacitors.

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4 50. The integrated device array of claim 47, wherein the devices
5 are capacitors and the device array forms part of a DRAM device.

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